Architecture and Filtering Requirements for Fully Digital Multi-radio Transmitters

Fabien Robert, Antoine Diet, Martine Villegas, Epifano Fabio, Cathelin Philippe, Triaire Pascal, Geneviève Baudoin

Architecture and Filtering Requirements for Fully Digital Multi-radio Transmitters

F.Robert[#*1], A.Diet[Δ], M.Villegas[2*], F.Epifano[#], Ph.Cathelin[#], P.Triaire[#], G.Baudoin[3*]

[*] *Université PARIS-EST, ESYCOM-ESIEE Paris, EA2552,*
ESIEE Paris, 93162 Noisy Le Grand, FRANCE
[1]robertf@esiee.fr, [2]villegam@esiee.fr, [3]baudoing@esiee.fr

[#]*ST-Ericsson*

[Δ]*UMR 8506, L2S-DRE, Université PARIS-SUD 11, CNRS, SUPELEC*
SUPELEC, Plateau du Moulon, 91192 Gif S/ Yvette, FRANCE

***Abstract*— This paper gives filtering requirements for an all-digital transmitter and identifies technical and technological challenges. Herein, we highlight trade-offs implied by such a transmitter. This work targets a flexible and low power consumption transmitter, taking into account advantages of sub-micron CMOS technologies. We focused on a multi-radio transmitter for cellular standards such as GSM, WCDMA and LTE for mobile applications. Simulation results point out the mandatory frequency replicas management caused by up-sampling process and the so needed filtering before emission to be dimensioned. Specifications of the filter to be design are given after an overall fully digital architectures study.**

I. CONTEXT

For the last years, wireless applications increased their demand on low power consumption and high data rate transfer in the frame of WLAN and WPAN mobile communications. To satisfy this demand, mobile terminals must be able to address different communication standards such as GSM, WCDMA and brand new LTE. The increasing number of cellular standards highlights the challenging development of multi-radio concept, for coexistence constraints. Coexistence implies the transmitter to be able to generate all different standard waveforms without over-sizing and increasing overall power consumption. In multi-radio the goal is to avoid transmitters parallelization, providing the ability to adapt a unique transmitter to several standards. This implies high flexibility at each stage of transmitter architecture. A classical direct conversion transmitter for mobile applications is shown in figure 1.

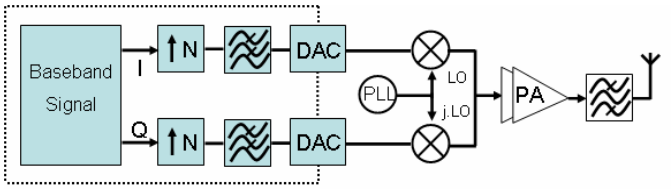

Fig. 1 Classical direct conversion transmitter

This transmitter architecture can be split into three different areas: digital baseband, analog baseband to RF and analog RF front-end. In this study we consider a cellular multi-radio transmitter supporting cellular communication standards (GSM, WCDMA and LTE). Transmit bands addressed will be 698 MHz to 915 MHz (bands 5, 8, 12, 13, 14, 18, 19) and 1710 MHz to 1980 MHz (bands 1, 2, 3, 4, 9, 10).

To design such a transmitter we must consider several parameters of the signal. Some parameters depend on the standard itself [1] [2] (and so modulation schemes) like bandwidth, power dynamic or envelope amplitude variation (also known as peak to average power ratio, PAPR). Other parameters directly depend on architecture like spectral purity, linearity or power efficiency. In a coexistence context, in the same terminal, spectral purity is a very important feature since emissions must respect standards limits and limit desensitization of other radio engines.

Theses limits are defined through adjacent channel power ratio (ACPR), adjacent channel leakage ration (ACLR) and transmit cellular spectrum emission masks setting co-existence with connectivity standards RX or duplex FDD cellular reception. Considering WCDMA standard as an example, we must respect at least -33 dBc ACLR1 and -43 dBc ACLR2. Consequently, the architecture in figure 1 leads to use "Digital to Analog Converters" (DAC) with more than 7 bits of resolution at hundred MHz clock rate.

Nowadays sub-micron technologies allow to design challenging solutions at a few GHz rate. Higher sampling frequencies lead to a larger frequency offset between LO and replicas. It then relaxes constraints on filtering key blocks along the signal path.

The goal of this study is to demonstrate the ability and benefit in pushing the Digital to Analog (D/A) frontier towards mixing or even power amplifying blocks. In the following part, we present three kinds of digitally based transmitter architectures. Theses examples are classified depending on their growing digitization degree, from the less digitized to the most digitized.

Then, we study main blocks of an all digital architecture: up-sampling, digital mixing and D/A conversion. Finally, we propose some solutions to improve replicas management due

to up-sampling and we specify the most important characteristics of the filtering block.

II. Digital Transmitter Architectures

Innovating baseband processors performances and research improvements on high speed DACs lead to integrate more and more transmitter key blocks in the digital domain. In this part we detail the evolution of the digital part in transmitter architectures from baseband toward power amplifier (PA).

A. Digital Mixing Architectures

Mixing is the first block, we can observe after up-sampling stage and FIR-IIR filters in a classical transmitter. The first architecture we present includes the mixing stage in the digital domain. Mixing an up-sampled baseband signal at GHz frequency implies transistors with a high cut-off frequency. Using 90 nm CMOS technology addresses this challenge. The architecture presented [3] [4] [5] is based on a classical direct conversion architecture. This architecture is digitized the closest possible to the PA. Frequency synthesis and power amplification stage are still analog blocks in this system. Figure 2 shows this architecture.

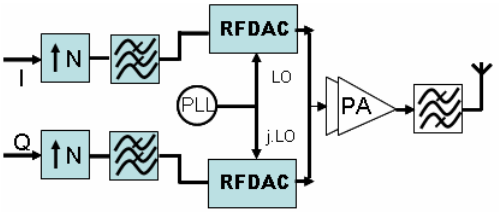

Fig. 2 Digital mixing architecture

Digitization of the mixing block limits process imperfections such as biasing path isolation leading to LO (Local Oscillator) leakage. It reduces the importance of using heavy calibration loops and so improves the overall system stability. It also reduces occupied area of the chip. In this architecture, mixing and D/A conversion are operated in a single block, the "RF Digital to Analog Converter" (RFDAC) (figure 2). It is important to note that up-sampling frequency and converter frequency must be chosen so that zeros of the SINC filter function (zero order hold: ZOH) match with baseband signal harmonics due to up-sampling. This architecture can be seen as a basis towards fully digital architectures although it still depends on analog frequency synthesis and power amplification. Power consumption implied by this new block can be highlighted as a drawback. This will be discussed in part III.

B. Digital Mixing and Frequency Synthesis Architecture

The second architecture [6] is also based on direct conversion architecture. It has been developed by a STMicroelectronics team for WiFi/WiMAX signals at 2.4 GHz. Compared to previous architecture many improvements were made. The "Sigma-Delta RFDAC architecture" (figure 3) presents the advantage of using digital blocks from baseband to the PA including an all digital phase lock loop.

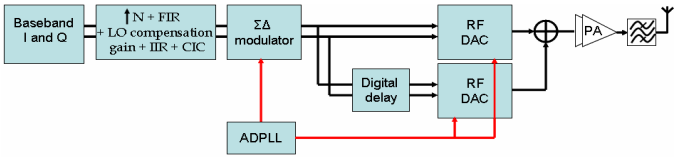

Fig. 3 Sigma-Delta RFDAC architecture

As in the previous architecture, baseband signal is up-sampled with filtering of oversampling replicas through FIR and IIR filters. As an improvement the signal gain control is performed throughout the overall transmission chain. The first power control appears just after up-sampling stage with a 12 dB "low speed" dynamic control.

This is done by multiplying IQ signals with a 10 bits control word. A second control "high speed" appears, with an additional range of 18 dB (using 6 dB steps). Until then, the signal is up-sampled to half the desired carrier frequency. MASH multi-bits ΣΔ modulators oversample both I and Q signals to twice the carrier frequency. Sub-microns technologies such as 65 nm CMOS allow this, since we need high speed (5 GHz) multi-bits modulators.

IQ signals are then separated: IQ and I'Q' paths. A delay is applied to I'Q' path. The combination of both mixed IQ and I'Q' after RFDACs generates notches in the spectrum noise shaping area. It helps reducing the TX shaping noise in a close-in RX band. Moreover, an additional 6 dB gain control is possible by shutting down the I'Q' RFDACs. The drawback is the suppression of the advantage of notches. It is possible only if shaping noise is below spurious emission limits in narrow bands.

C. Fully Digital Architecture

The last architecture [7] (figure 4) is the most digitized one. The "Digital Quadrature RF Modulator" (DQRM) is based on a digital IQ approach architecture. As well as in [3] and [6], IQ signals are up-sampled and filtered. This is done in order to place spectral re-growths (ZOH) far enough from the carrier frequency. This is possible, setting notches at multiples of the oversampling frequency. Two signals are created "abs(I+Q)" and "abs(I-Q)". This two signals are coded through a thermometer coder and alternatively fed at the input of a Digitally-driven Power Amplifier (DPA) at twice the LO frequency.

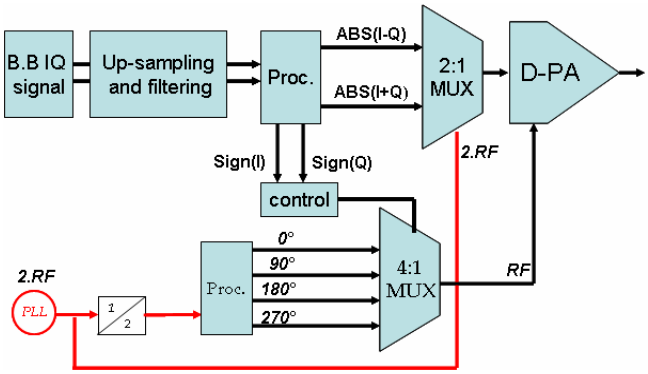

Fig. 4 DQRM architecture

It can be seen as an oversampling by four of the envelope signal. Moreover signs of "I+Q" and "I-Q" are calculated to estimate the phase information, and to create four phases control digital words. Theses words activate at each change of IQ symbol, one of the four 90° phase shifted clock signal at the carrier frequency. Thus, each time IQ symbols change, the phase of the carrier frequency changes. Phase and amplitude are recombined through the DPA comparable to a RFDAC. Taking the example of an 8 bits binary to thermometer coding, this will lead to use 256 pairs of transistors, each providing a unit current source.

Amplitude takes two values at 2 x RF frequency, and the clock alternates positive and negative current sources in the DPA at RF frequency. It results in the following samples at each symbol: abs(I-Q) abs(I+Q) -abs(I-Q) -abs(I+Q). Bandpass filtering at the output helps to restore the initial signal. As we obtain a NZR signal, filtering is less stringent than when using a classical IQ modulator. DPA behaviour will be detailed in part III. This architecture has the advantage of frequency flexibility although up-sampling ratio must be adapted to the carrier frequency. This depends on the targeted band at the emission due to proximity of other RX standards bands. The principal issue in frequency reconfigurability is to find a filtering solution associated to the DPA. It is also well power flexible thanks to the biasing of each unit current source transistor. In [7] an example is given at 5.8 GHz for a WiMAX signal of 10 MHz (64-QAM) which is very tough. Resulting spectrum re-growths in theses conditions are less than -50 dBc/Hz.

III. KEY FUNCTIONS OF A DIGITAL TRANSMITTER

This paragraph will detail the main functions we have to deal with in the design of a fully digital transmitter. These are the digital up-sampling stage, and the digital mixing D/A conversion and power amplification stage.

A. How up-sampling impacts on filtering?

Every partially or fully digital transmitter has an up-sampling stage to increase SNR before carrier mixing. As we show below a trade-off must be done between up-sampling frequency, IQ quantization number of bits and post mixing filtering. Up-sampling replicas appear in the spectrum. We can define a ratio (UF) between Transmit frequency (F_{RF}) and up-sampled baseband frequency ($F_{upsampling}$).

$$UF = \frac{F_{RF}}{F_{upsampling}}$$

Several parameters related to the architecture and signal affects replicas behaviour. These are the signal bandwidth, the up-sampling factor and the number of bits used to quantify I and Q signals. Figure 5 illustrates the spectrum obtained at the output of an all digital architecture. Signal is a 20 MHz LTE (64-QAM) at F_{RF}=2 GHz. Up-sampling frequency is set to 200MHz.

As an illustration of number of bits impact on close band noise, the architecture was simulated using 7 bits (red) and 15 bits (blue) resolution for IQ.

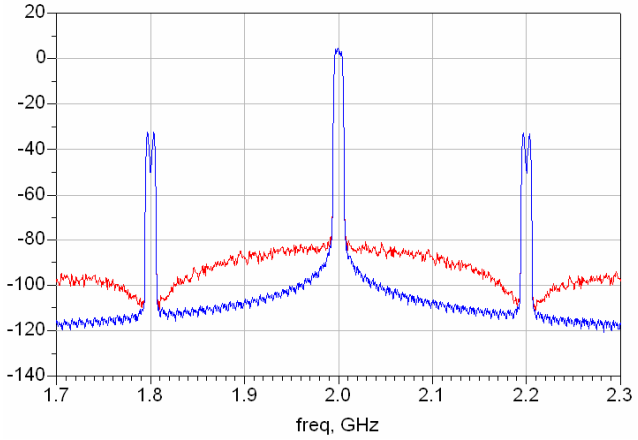

Fig. 5 All digital architecture output spectrum

We observe in this figure notches at the centre of replicas frequencies implied by the convolution of signal with SINC² interpolation function of the up-sampler (ZOH). The lower the signal bandwidth, the lower are replicas level. We made simulation for LTE 20, 10 and 5 MHz bandwidth (still 2 GHz F_{RF} and UF = 10).

TABLE. I Impact of signal bandwidth on replicas level

Signal Bandwidth	1st replicas (dBc)	2nd replicas(dBc)
20MHz	-33,7	-39,8
10MHz	-40,4	-46,4
5MHz	-47,7	-53,4

In the case of a GSM 900 signal replicas level decreases to -81 dBc which is lower than the standard requirements of -69 dBc. In a multi-radio context large bandwidth standards (LTE, WCDMA) will be a constraint over replicas level.

This table shows the impact of up-sampling on spurious emission at a frequency offset corresponding to $F_{upsampling}$. As a second step we simulate the impact on close band noise while moving quantization resolution from 5 to 15 bits.

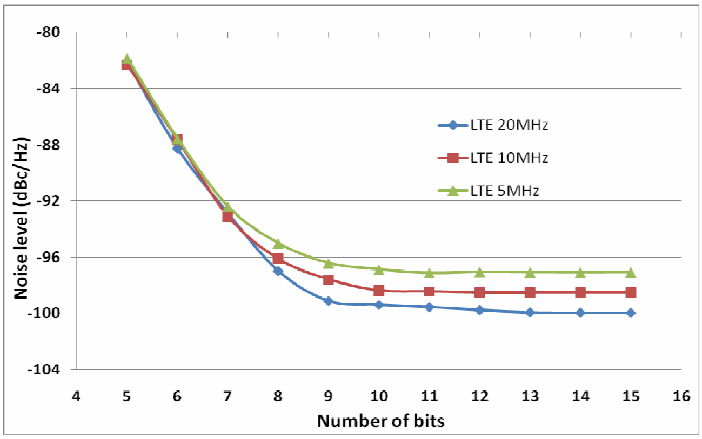

Fig. 6 Impact of IQ resolution on Tx band close noise

On figure 5, we plot a comparison of architecture signal output spectrum between 7 bits and 15 bits resolutions to observe the impact in quantization number of bit. Looking at figure 6, we observe a reduction of close noise level as the number of bits increases. It exists some solutions to artificially increase signal resolution up to 13 bits [8]. Finally the third mean leading to an optimisation of replicas is the ratio UF between F_{RF} and $F_{upsampling}$. The higher is $F_{upsampling}$, the lower is UF and further apart are replicas, thus relaxing filtering.

Sub-micron technology now helps to up-sample at hundred MHz rates. Simulations were done to estimate performances while increasing $F_{upsampling}$ (case of GSM 900), and are reported in figure 7.

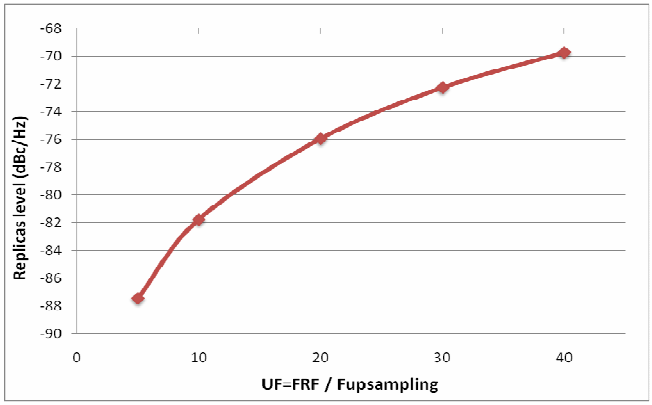

Fig. 7 Impact of up-sampling frequency on replicas level

As UF decreases, replicas are pushed away from the emission band. This helps to reduce complexity of the final filtering stage. Looking at each TX band spectrum emission mask, we must be careful with spurious emissions that could desensitize Rx band (FDD case) and also other standards Rx such as GPS in the same terminal.

The most stringent coexistence band is the GPS limiting emissions of other standards to -168 dBm/Hz. To be sure every replica is filtered enough we have to characterize the worst case. Our simulations showed the worst case (if UF=10) is for WCDMA TX band 4 with 66dB attenuation needed at 129MHz from the carrier. This is quite difficult to obtain, so we need to optimize replicas placement in spectrum to relax filtering constraints. This will be detail in part IV.

B. Digital to analog mixing toward power amplification

As the signal is up-sampled at the right frequency to minimize level of replicas, it must be mixed around the carrier. This digital signal must be D/A converted using DACs of at least 7 bits resolution (see previous paragraph). In fully digital transmitter this two steps can be done in the same block using an RFDAC [3][4][5][6] .

The principle is the parallelization of weighted or unit Gilbert cells activated by the amplitude signal codeword. The data is coded by an N-bits word depending on the expected DAC resolution. Figure 8 represents an example for a 4 bits coded signal.

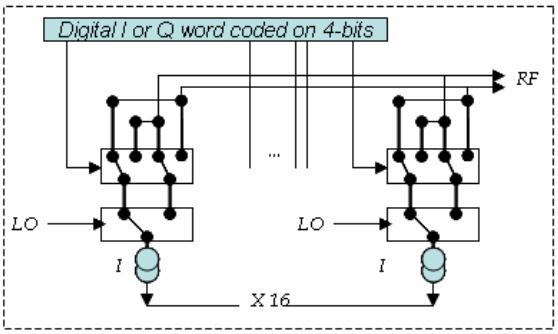

Fig. 8 RFDAC example

At the LO rate, switches activate the parallelized unit cells, providing unit current sources depending on the codeword. Final current is then proportional to amplitude level of I or Q up-sampled signal. The linearity and the resolution of the signal increase as parallelized cells increase. Parallelization smooths IQ imbalance and results from the average cells imbalances. Power control of the structure can be done by a variation on the bias current, resulting in a reduced output current of each unit cell. Some realizations show 9 bits RFDAC able to perform 45 dB power control [7].

RFDAC design depends on the kind of signal to transmit. In nowadays cellular context we transmit high PAPR signals in HSUPA (7.3 dB on RF, 9.6 dB on IQ path) so we need to adapt current cells weight. As an example if baseband signal is on 10 bits, the 4 LSB bits are coded into a 16 values thermometer code to control 16 unit current (I) cells. On the other side the 6 MSB are coded into a 64 values thermometer codeword to drive the 64 weighted (16 x I) current cells. A major issue of RFDAC is the RF power they are able to provide. If targeting standards such as GSM, transmitter must emit up to 33dBm. Recent work [9] shows RFDAC providing a maximum of 2.7 dBm. This introduces the question of how providing more power while keeping advantages of RFDACs.

The concept of DPA for Digital Power Amplifier appears. This can be seen as a digitally modulated PA. Instead of parallelizing current cells, DPA parallelizes unit PAs. Depending on an amplitude codeword, amplifiers are fed by the phase modulated signal to be amplified. The maximum power obtained with this solution, reaches 25 dBm peak [10]. A weakness of this concept is to dynamically match the DPA impedance with the antenna load while switching unit PAs (load pull effect).

IV. IMPROVEMENT

In the previous paragraph we showed two main drawbacks of fully digital transmitters. First one is the quantization noise close to the emission bandwidth, second are replicas due to up-sampling. At less than $F_{upsampling}$ offset from TX band, the most limiting factor is the quantization noise polluting RX band. This can be corrected by increasing the number of bits up to 7 to satisfy at least -90 dBc as presented in figure 6. At more than $F_{upsampling}$ from TX band, main spurious contributors are replicas from up-sampling. From this hypothesis we first evaluate filtering requirements, trying to respect both WCDMA and LTE spectrum emission masks.

DQRM architecture was simulated assuming an output power of 10dBm which is the targeted power in nowadays fully digital architecture. We show below on table II, requirements at the antenna for the two most stringent bands (band 1 and 4). Band 4 is very stringent due to GPS band.

TABLE. II Filtering requirements at antenna function of UF

				Attenuation (dB)	
Band	Standard	Target PSD (dBm/Hz)	freq offset from LO (MHz)	UF=5	UF=10
1	WCDMA	-125.8	40	29	22
1	LTE	-110	40	13	6
4	WCDMA	-168	129	76	66
4	LTE	-168	129	76	66

For the replicas not to desensitize simultaneously operating receivers, we must set replicas power level at the minimum power level admitted in theses bands. If looking at band 1 we must be careful to set out of band emissions to target a maximum level of -140 dBc/Hz in own FDD cellular Rx band and -125.8 dBm/Hz spurious emission level at antenna elsewhere. If transmitting WCDMA with UF=10, this leads to a 29 dB filtering at 40MHz from the carrier frequency. Looking at band 4, to respect co-existence with GPS band (-168 dBm/Hz) we must assure a 66 dB filtering at 129 MHz from the carrier. This is very difficult to implement.

This implies very stringent and quite impossible filtering at the output of the architecture before the last stage of power amplification. Assuming that the most limiting parameters for replicas power level are other standards Rx bands we can imagine a replicas management process. The main idea is to evaluate the optimal up-sampling frequency for each cellular Tx band avoiding to place replicas in other standards Rx bands. Thus replicas power levels are only defined by the spectrum emission mask of the emitted standard. Below on figure 9 is represented the example of LTE band 1 using a 5 MHz bandwidth. We have chosen a clever up-sampling frequency placing the first replica far from band 33 and just below the GPS band thus drastically reducing filtering requirements.

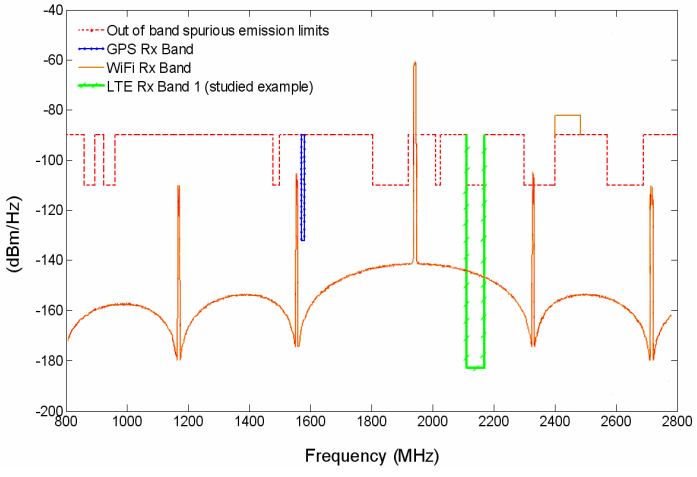

Fig. 9 Spurious Emission Mask for 5MHz LTE band 1 versus DQRM Tx Spectrum at 10dBm output power (normalized in dBm/Hz)

The same process was applied to all cellular standards Tx band. As we must keep in mind that this architecture has to be designed we choose optimal up-sampling frequencies that are integer multiples of dedicated carrier frequency. This leads to re-evaluate the previous table filtering requirements.

TABLE. III Filtering requirements at antenna after replicas management for the same study case

Band	standard	Target PSD(dBm/Hz)	Freq offset from LO (MHz)	Attenuation (dB)
1	WCDMA	-125.8	390	20
1	LTE	-110	390	5
4	WCDMA	-125.8	360	23
4	LTE	-110	360	7

Looking at band 1 and 4 WCDMA the most difficult case is to obtain 23 dB attenuation at 360 MHz from LO.
Now we can define a precise filter design goal to achieve requirements for every cellular Tx standard considering all digital transmitter architecture. Moreover if we want to address all theses bands, we must have a certain frequency tuning agility. We can split the problem in two different agile filters. The first one would address low frequencies from 698 MHz to 915 MHz (bands 5, 8, 12, 13, 14, 18, 19) and the second would address high frequencies from 1710 MHz to 1980 MHz (bands 1, 2, 3, 4, 9, 10).

For both filters goal were set as follow:

- 23dB attenuation at 360MHz from center frequency
- 3dB bandwidth of at least 60MHz

First obtained results in filtering topologies synthesis leads us to use high quality factor elements (Q > 500).

V. Future Works

In the multi-radio context, we identified some limitations if using fully digital transmitter architectures for cellular standards. We demonstrated some keys to meet cellular standards requirements.

This can be achieved if respecting above given system specifications and filtering requirements. This method can be applied for all fully digital architectures since replicas management is a global issue for this kind of architecture. In our cellular multi-radio context the most challenging specifications to address are high resolution DACs at GHz frequencies and architecture output filtering. Managing replicas level through a clever choice in up-sampling frequency help to relax filtering specifications.

We showed the most challenging case for WCDMA Transmit band 4 (23 dB attenuation need at 360 MHz from LO) using a 7 bits resolution. After these simulated results, a solution is currently in development for reconfigurable high band and low band filters addressing Transmit bands from LTE band 12 (698 MHz) to WCDMA band 1 (1980 MHz) using high Q elements.

REFERENCES

[1] LTE and WCDMA standard specifications: 3GPP TS 25.101 V9.1.0 (2009-09).

[2] GSM / EDGE standard specifications: 3GPP TS 45.005 V8.3.0 (2008-11). 3rd Generation Partnership Project; Technical Specification Group GSM/EDGE; Radio Access Network; Radio transmission and reception (Release 8).

[3] P. Eloranta et al., "A multimode transmitter in 0.13 μm CMOS using direct-digital RF Modulator," *IEEE J. Solid-State Circuits*, vol. 42, pp. 2774–2784, Dec. 2007.

[4] A. Jerng, C. Sodini, "A Wideband Sigma Delta RF Modulator for High Data Rate," *IEEE J. Solid-State Circuits,* vol. 42 N°8, Aug. 2007.

[5] P. Eloranta et al., " Direct Digital RF Modulator: a multi-function architecture for a system-independent radio transmitter," *IEEE Communication Magazine*, vol. 46, Issue 4,pp. 144-151, Apr. 2008

[6] A. Pozsgay et al., "A Fully Digital 65nm CMOS Transmitter for the 2.4 to 2.7 GHz WiFi/WiMAX bands using 5.4GHz Sigma Delta RF DACs," *Solid-State Circuit Conference, ISSCC 2008, Digest of Technical Papers. IEEE International*, pp. 360-619, Feb. 2008.

[7] VK. Parikh et al., "A fully digital architecture for wideband wireless transmitters," *Radio and Wireless Symposium, 2008 IEEE*, pp.147-150, Jan. 2008.

[8] VK. Parikh et al., "All Digital Quadrature Modulator Based Wideband Transmitters" *IEEE Transactions on Circuits and Systems regular paper*, vol 56, issue 11, pp. 2487-2497, Nov. 2009

[9] J. Gutierrez et al., " A 1.4GS/s 9-bits 45dB Power Control RFDAC for Digital Radio Transmitters.", *Analog Integrated Circuits and Signal Processing, Springer Netherland*, Jul. 2009

[10] S. Pornpromlikit et al., "A 25-dBm High-Efficiency Digitally Modulated SOI CMOS Power Amplifier for Multi-standard RF Polar Transmitters.", *IEEE Radio Frequency Integrated Circuits Symposium, RFIC 2009*, pp. 157-160, June. 2009